AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning on line 22 of page 1, as follows:

Digital signal processing, including the processing for spread-spectrum wireless communications makes considerable use of digital filters. Digital filtering involves processing of sampled-data, or discrete-time, signals in ~~accord~~ accordance with a filtering algorithm. Stated another way, a digital filter utilizes a computational process, carried out either through dedicated hardware or through the execution of a sequence of instructions by programmable logic, by way of which an input sequence of numbers representing discrete signal samples is converted into an output sequence of numbers, modified by the transfer function of the desired filter.

Please amend the paragraph beginning on line 24 of page 4, as follows:

Hence, one aspect of the present ~~invention relates~~ teachings relate to a method of digital filtering of a digitized input stream in ~~accord~~ accordance with an intended filter function. The intended filter function may be approximated as: a sum of products of a series of one or more first coefficient values and a series of one or more samples from a digital output stream; added together with a sum of products of a series of one or more second coefficient values and a series comprising a one or more samples from the digital input stream. The ~~inventive~~ method involves combining predetermined sets of one or more samples from the digital input stream with one or more samples from a digital output stream, to form a plurality of respective numeric input values. Each respective numeric input value is scaled, by a different power of the base numeric value used for the digital filtering. In a digital filter implemented in binary form, each scaling involves shifting the respective input value so as to modify the input value as if it were multiplied by an appropriate power of two. The scaling, however, can be implemented as a simple shift function, without using a numeric (e.g. fixed-point) multiplication operation. The

resulting scaled values are added together, to form a digital output stream in ~~accord~~ accordance with the predetermined filter function.

Please amend the paragraph beginning on line 19 of page 6, as follows:

Fig. 2 is a simplified functional block diagram of an embodiment of a digital filter ~~in accord with the present invention~~.

Please amend the paragraph beginning on line 23 of page 6, as follows:

Fig. 4 is a simplified functional block diagram of an embodiment of a digital filter providing the same filter transfer function as Fig. 3 but implemented in ~~accord~~ accordance with an embodiment of the present ~~invention~~ teachings.

Please amend the paragraph beginning on line 19 of page 9, as follows:

The scalers 33^{L_1} to 33^{L_2} supply the scaled values to an adder 35, which totals all of the scaled values to form the output signal *y(n)*. During each clock cycle, the output value *y(n)* is a computed sample value derived by the computations performed by the digital filter circuit 30, in ~~accord~~ accordance with the desired filter function and implemented in ~~accord~~ accordance with the ~~invention as shown~~ the illustrated example.

Please amend the paragraph beginning on line 14 of page 11, as follows:

In ~~accord~~ accordance with the ~~invention~~ present concepts, it is possible to replace the fixed-point multiplications of sample values with simple connections corresponding to binary (1 or 0) coefficient values in combination with appropriate scaling operations. Consider now an

application of the ~~invention~~ technique to the same filter function. First, the coefficients 0.875 and 0.375, from the simple example can be expressed in binary form as follows.

Please amend the paragraph beginning on line 18 of page 12, as follows:

There is 1 adder needed for $y(n-1)+x(n)$; and 2 adders needed to combine $y(n-1)\cdot 2^{-1}$, $(y(n-1)+x(n))\cdot 2^{-2}$ and $(y(n-1)+x(n))\cdot 2^{-3}$ together. Therefore, 3 adders are needed to implement $y(n-1)\cdot 2^{-1}+(y(n-1)+x(n))\cdot 2^{-2}+(y(n-1)+x(n))\cdot 2^{-3}$. We save 1 adder compared with the direct method. This is a very simple example. In many real digital filters, many more bits and many more multipliers would be required, and therefore the savings on hardware due to use of the ~~invention~~ present teachings is huge. This inventive filter function can be implemented in a digital signal processor or in hardware. Fig. 4 shows a functional representation of the inventive filter processing. These functions may be implemented as process steps performed in the digital signal processor. For discussion of a presently preferred embodiment, the block diagram represents a hardware implementation 50 of this simple digital filter function in ~~accord with the invention~~ accordance with an example.

Please replace page 20, containing the abstract, with the new version thereof shown on the following separate page: